

Group “Smallest Transistor” – Review Papers Summary

1. Vazquez-Mena et al. Resistless nanofabrication by stencils: A review

The paper reviews stencil lithography, a resistless technique using stencils for shadow masking a flux of atoms, molecules or particles, to modify the substrate surface by methods such as deposition, etching, or ion implantation - without conventional photoresist. Stencil lithography does not require resist processing, making it compatible with a broad range of material substrates, as well as with deposition of sensitive materials, and the stencil is in general not in direct contact with the substrate preserving fragile substrates, which are key advantages for MEMS/NEMS.

Stencil lithography avoids photoresists, solvents, and radiation, enabling safe fabrication on fragile or chemically sensitive substrates such as membranes, cantilevers, and pre-processed CMOS wafers.

Rigid masks (Si, SiN) suffer from challenges like stencil–substrate gaps and fragility. Flexible masks (PDMS, parylene, polyimide) improve conformity to non-planar or curved substrates, reducing blurring and broadening the scope of possible applications.

The main challenges are blurring, caused by stencil–substrate gaps and surface diffusion, which can be mitigated with compliant membranes, supports, gases, or etching, and clogging from material buildup, which can be reduced by coatings, heating, or cleaning.

SL supports diverse applications, including plasmonics (nanodots, gratings for solar cells, biosensors), electronics (thin-film transistors, graphene/CNT contacts, CMOS devices), biotechnology (protein and cell patterning), and MEMS/NEMS (cantilevers, sensors, nanoresonators, NIL stamps).

Its reusability makes SL cost-effective, and full wafer-scale demonstrations show its potential not only for prototyping but also for scalable MEMS/NEMS manufacturing.

The paper was published in 2014. Since then there is only one review paper published ‘Stencil Lithography for Scalable Micro- and Nanomanufacturing’ in 2017. (Du, K., Ding, J., Liu, Y., Wathuthanthri, I. and Choi, C.H., 2017. Stencil lithography for scalable micro-and nanomanufacturing. *Micromachines*, 8(4), p.131.)

The review includes numerous figures and schematics (e.g., stencil fabrication, blurring effects, SEM/AFM images, dynamic patterning) demonstrating a strong compilation of data. It provides a clear and detailed discussion of the topic across materials, techniques, challenges, and applications.

2. Howell et al. Thermal Scanning Probe Lithography: A review

Thermal Scanning Probe Lithography is a maskless technique where extremely high-resolution (<10nm) can be achieved. It employs a heated probe to locally modify a resist or substrate. Its flexibility in producing both 2D and 3D patterns with high precision makes it relevant for

MEMS and NEMS, where complex geometries, rapid prototyping, and minimal process-induced damage are critical for device performance and integration.

Sub 10nm resolution with direct writing ability: maskless technique where direct patterning is possible. 3D structures due to precise depth control: conventional photolithography allows precise 2D geometries, while t-SPL guarantees excellent depth control. Ability to operate with a wide material range: different photoresists can be employed. Reduced thermal and chemical damages: localized heat lowers the damages and helps fabrication on sensitive substrates.

As a future outlook of the technique, even though its main limitation is the limited throughput, which pose a question on its industrial applications, authors see hybrid t-SPL, where direct laser writing and t-SPL are combined, as a potential solution to boost the throughput and achieve a rapid prototyping ability. Moreover, an industrial application can be represented by its use for modifications of small critical areas of a device.

Review paper from 2020. Yes, there are newer papers. Most of them are on SPL techniques, where t-SPL is just briefly mentioned. While Here the list in chronological order:

- Albisetti, E., Calò, A., Zanut, A. et al. Thermal scanning probe lithography. *Nat Rev Methods Primers* 2, 32 (2022). <https://doi.org/10.1038/s43586-022-00110-0>
- J. Gao, W. Xie, X. Luo, Advanced electrical and thermal scanning probe lithography for next-generation nanodevice fabrication. *Proceedings Volume 13427, Novel Patterning Technologies 2025; 1342703* (2025) <https://doi.org/10.1117/12.3049277>

The review paper looks really complete. Even for someone not expert of the topic, the description is really accurate and figures help understanding both the fabrication process and the applications that it has.

3. Mastrangeli et al. Self-assembly from milli- to nanoscales: methods and applications

The paper (2009) reviews self-assembly techniques across scales, highlighting their growing relevance for MEMS and NEMS. Self-assembly is important in two main ways: (i) as a packaging alternative, it enables parallelization, higher throughput, and compatibility with shrinking feature sizes and heterogeneous materials; (ii) in MEMS fabrication, it supports aggregation of parts, folding, and 3D structure assembly, which are difficult with purely top-down methods.

Key takeaways are: (1) self-assembly provides a pathway to continue downscaling while maintaining yield; (2) the diversity of mechanisms (capillary, magnetic, chemical, biological) makes it versatile for different processes and applications; (3) hybrid approaches that combine top-down patterning with self-assembly are especially promising; (4) despite intense research, the theoretical understanding is still fragmented; (5) the outlook points toward algorithmic and programmable self-assembly, which could impact computing, molecular design, and predictive modeling.

The review has been widely cited since publication, including in recent work (Nanophotonics 2023; 12(6): 1019–1081, and Nature 624, 57–63 (2023)) and newer reviews (Annu. Rev. Control Robot. Auton. Syst. 2019. 2:181–203, and Adv. Mater. 2020, 32, 1902994). Its quality is strong, with a thorough survey and a useful summary table, but it lacks concrete examples of large-scale industrial adoption (beyond some packaging demonstrations) and includes few original figures. Overall, it remains a well-regarded, influential academic review.

4. J. Alexander Liddle et al. Lithography, metrology and nanomanufacturing

This paper reviews the role of lithography and metrology in nanomanufacturing, with emphasis on the semiconductor industry. IC fabrication requires extreme precision: features below 40 nm must be controlled within a few nanometers and aligned across many layers. This is possible through optical lithography at 193 nm combined with immersion, double patterning, and continuous metrology. Because ICs are very high value, such costly infrastructure is justified. However, this model cannot be applied to lower-value applications like flexible electronics, photonics, or biomedical devices.

The review compares top-down and bottom-up approaches. Optical lithography faces a fundamental “triangle of death” trade-off between sensitivity, line edge roughness, and resolution. Electron and ion beams reach high resolution but throughput remains a bottleneck. Scanning probe methods achieve atomic control but are impractically slow. Nanoimprint lithography avoids some of these limits but suffers from defect generation and overlay errors. On the other hand, self-assembly methods such as block copolymer ordering or DNA origami are low-cost and produce dense patterns, yet they lack deterministic placement and structural hierarchy. Directed self-assembly offers a compromise by combining top-down templates with bottom-up ordering, but defectivity remains an open issue.

Metrology is identified as a critical enabler. In ICs, expensive SEM based metrology is affordable, but for cheaper nanoproducts it is not. Future manufacturing requires new approaches that are both faster and less costly, such as scatterometry, X-ray diffraction, or light scattering. The paper suggest the need to balance slow and detailed process development with high speed and real time monitoring during production.

For the future, the paper highlights three open challenges: scalable and defect-tolerant patterning, device designs that can tolerate imperfections, and cost efficient metrology. Without much advancement in these areas, many nanotechnology applications risk remaining at the research stage instead of reaching industrial adoption.

5. L. Vestraete et al. Enabling chemically amplified resists towards tight pitch EUV patterning by directed self-assembly

Directed self-assembly (DSA) combined with chemically amplified resists (CARs) for tight-pitch EUV lithography patterning. Relevance for MEMS/NEMS: Advanced MEMS/NEMS require high-resolution, low-variability nanostructures for sensors, actuators, and memory devices. This work shows how integrating DSA with EUV lithography improves line width

roughness, pattern placement accuracy, and defectivity at sub-30 nm scales. Such approaches directly support the scalable fabrication of nanoscale features critical to MEMS/NEMS performance and reliability.

The paper demonstrates that DSA + CAR synergy can extend EUV lithography limits, relevant for advanced memory (e.g., DRAM capacitor arrays) and logic scaling. Highlights open questions on the origin of LER and the trade-off between film thickness and ordering kinetics.

For 24 nm L/S, best stack = SiCN/aC, with high- χ BCP further lowering LWR, though LER remained stack-limited. For 30 nm HEXCH, thicker BCP films reduce LPPE, while high- χ BCP improves LCDU, LPPE, and defectivity. High- χ BCPs are critical for next-generation high-precision patterning.

6. Young Rag Do et al. MicroLEDs get in line

Topic: Fluidic-assisted self-alignment of MicroLEDs via surface roughness control. Relevance for MEMS/NEMS: Demonstrates scalable assembly using surface forces and fluidics, offering strategies for integrating micro/nano devices and enabling cost-effective large-area system fabrication. Chips are engineered with different surface roughness on opposite sides: Smooth AlN side (strong van der Waals force) → bonds well to the substrate. Rough metal electrode side (weak force) → prevents incorrect bonding. Chips suspended in solvent are spray-coated onto the substrate, then swept with an alignment bar. The sweeping process flips and aligns the chips, bonding them in the correct orientation.

This article reviews a fluidic-assisted self-aligning transfer method, which leverages chip surface roughness to control van der Waals bonding for high-yield, large-area MicroLED alignment, demonstrating functional display prototypes but facing ongoing challenges in resolution scaling, chip damage control, and material performance.

Key (3-5) take away messages from paper:

- Exploiting surface roughness differences → controls van der Waals interactions for correct orientation.
- Simple and cost-effective → more feasible than conventional transfer techniques.
- High-yield, large-scale alignment → demonstrated on an 8-inch silicon wafer

Limitations and Future Challenges:

- Scaling resolution and display size → requires deeper study of fluidic control parameters.
- Chip damage → must be minimized during transfer to maintain efficiency.
- Material constraints → current GaN-on-silicon technology shows inferior optical/electrical performance compared to GaN-on-sapphire; future improvements may involve defect-free GaN-on-silicon using 2D materials (e.g., single-crystal graphene).